Microfabrication

SOFIA RAHIMINEJAD

Department of Microtechnology and Nanoscience, MC2
CHALMERS UNIVERSITY OF TECHNOLOGY
Göteborg, Sweden, 2014

Compendium of

Microfabrication processes

SOFIA RAHIMINEJAD

Department of Microtechnology and Nanoscience
CHALMERS UNIVERSITY OF TECHNOLOGY
Göteborg, Sweden 2014

Contents

List of Figures

Chapter 1

Introduction

Microfabrication is the technology of constructing and manipulating structures at a micrometer (10^{-6} m) scale. This handbook is intended as a toolbox of different methods and processes that can be used in microfabrication. There are four areas of microfabrication; Deposition or growth, adding/growing a material to an existing surface, Lithography, patterning a surface with a film, Etching, removal of material and Doping, modification of electrical properties, together they are all that is needed to create any structure or device. Microfabrication can be divided into two categories, surface micromachining and bulk micromachining. Surface micromachining only modify the wafer on the surface. By patterning different layers of oxide and metal films together with doping, electrical circuits such as transistors can be fabricated. Surface micromachining operates mostly in 2D. Bulk micromachining is a 3D process where also the wafer itself is modified. Etching deep into silicon is a typical bulk micromachining process. Bulk micromachining is often used in MEMS (Microelectromechanical systems) and its subcategories such as: MOEMS (Micro-Opto-Electro-Mechanical System), Microfluidics and RF MEMS. Some of the processes presented here have data taken directly from the MC2 cleanroom at Chalmers University of Technology so that the student can use real data.

Chapter 2

Lithography

In micromachining, lithography is the process used to pattern a wafer. Lithography is one of the basic and most common process in microfabrication. There are several steps used involved in patterning a wafer as can be seen in figure 2.1. Some of the steps involves processes explained in other chapters and are therefore referenced to those chapters.

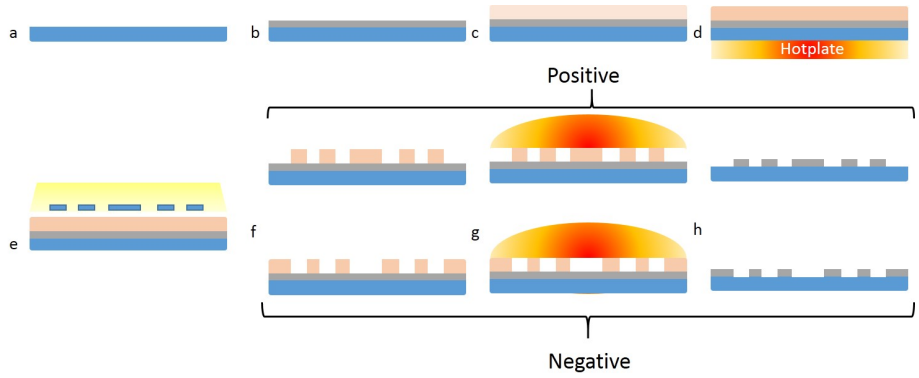


Figure 2.1: The process flow for lithography. First we have a substrate a), then the barrier layer is deposited b), the photoresist is spun on top c) and then the wafer is soft-baked d). The photoresist is then exposed with a chrome mask e), depending if the resist is negative(bottom row) or positive (top row) the photoresist will be stronger or weaker from the exposure. After exposure the photoresist is developed f) and hard-baked g). Finally the barrier layer is patterned and thereafter the photoresist is removed h).

2.1 Barrier Layer

A barrier layer (figure 2.1a) is a thin-film of SiO_2, Si_3N_4, polysilicon, metal or even photoresist, different processes to deposit a thin-film are explained in chapter 5. The barrier layer can be used for its material process as a component on a chip or as a so

called hard mask which can protect the substrate surface from etching or expose part of the surface for doping (chapter 4).

2.2 Photoresist deposition

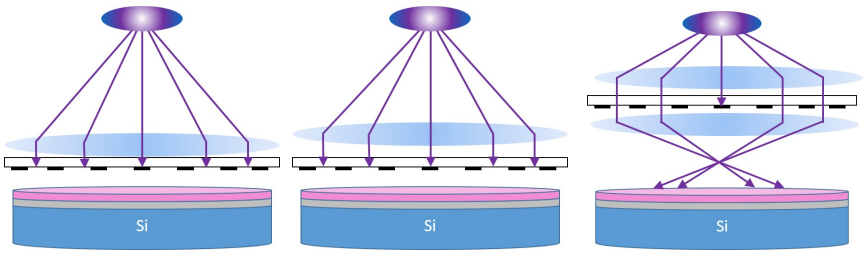
The wafer is placed on a spinner, which is a high speed rotating chuck and is used to deposit photoresist evenly on the wafer, in the MC2 cleanroom the Lapin from SUSS MicroTec group is one of the machines used. The thickness of the photoresist depends on the rotation speed of the chuck, the duration time and the viscosity of the photoresist. For example, the photoresist AZ4562 to achieve a thickness of about 7 μm, the wafer needs to be spun at 3000 rpm for 30 sec. First a primer, HMDS is applied to the wafer and spun to enable the stiction of the photoresist. The photoresist is then dispensed onto the wafer with the help of a pipette. A rule of thumb is 1 *ml* of photoresist per inch of the wafer diameter, a 4" wafer needs 4 *ml* of photoresist (figure 2.1c).

2.3 Soft Baking

Soft baking or pre-baking is when the wafer is heated to evaporate the solvent and enhance adhesion, figure 2.1d. This can be done on a hotplate or in an oven. The time and temperature depends on the photoresist and is always noted in the data sheet of the photoresist. Most commonly a hotplate is used so that the wafer is only heated from one side, allowing the solvent to evaporate at the top.

2.4 Alignment and Exposure

The desired pattern is first patterned on a chrome coated glass or quartz plate with the help of a laser e-beam maskgenerator and photoresist. The patterned chrome is called a photo-mask, this is what is used to define the pattern on your wafer. When illuminating your photo-mask with UV-light the clear areas will let the UV-light through and expose the photoresist on your wafer below. Depending if the photoresist is negative or positive the polymers in the photoresist will bind stronger respectively their bonds will break when exposed to UV light, figure 2.1e and f. The exposure time depends on the photoresist but also on the underlying materials properties. The exposure time needs to be optimized for the desired process, if the exposure time is too long the pattern will be overdeveloped and if the time is too short the pattern will be underdeveloped. For AZ4562 the standard exposure time is about 40 sec. There are three modes for the UV lens, contact, proximity and projection, figure 2.2. Contact mode (figure 2.2a) is when the UV lens is in direct contact with the photo-mask and gives the best resolution, however this can wear out the chrome pattern. To avoid this proximity contact (figure 2.2b) can be used, the scale will still be 1:1 but the resolution will decrease somewhat. Projection mode (figure 2.2c) can scale down the pattern on the wafer from the pattern on the photo-mask by using another UV lens between the photo-mask and the wafer. If several photomasks are used, alignment marks are needed. They are used to align a photo-mask to an already existing pattern on the wafer from a previous lithography step. Examples of alignment marks can be seen in figure 2.3.



(a) Contact mode (b) Proximity mode (c) Projection mode

Figure 2.2: Different modes for the UV lens.

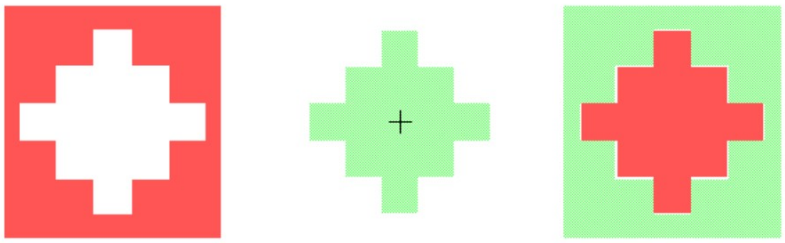


Figure 2.3: Alignment marks. To the left is the pattern on the wafer. In the middle is the pattern on the photo-mask and to the right are two marks aligned above each other.

2.5 Development

The weakened areas after UV exposure will then be easier dissolved with an alkaline, i.e. the developer. When developing, the time in the developer is the main factor to consider, depending on the photoresist, some agitation is needed. If developed too long the pattern will be overdeveloped and the open spaces will be bigger this also happens if the wafer is agitated to much. If the developing time is too short or the wafer is not agitated enough, the pattern will be underdeveloped and the open spaces will be smaller than desired. A standard developing time for AZ4562 is about 3 min. After development the wafers needs to be rinsed and dried. The wafer is then inspected in a microscope and if the results are satisfactory then one can proceed to the next step.

2.6 Hard Baking

When the development is satisfactory the wafer needs to be hard baked, most commonly in an oven but it can also be hard baked on a hot plate, figure 2.1g. This step will harden the photoresist and improve adhesion. Thereafter the barrier layer can be patterned (figure 2.1h) through dry or wet etching (see chapter 6) and then the photoresist is removed in a solvent.

Chapter 3

Oxidation

Oxidation is the process where a layer of SiO_2 is formed on a Si surface by exposing the Si to oxygen. Si reacts very easily and there will always be a thin layer of SiO_2 when Si is exposed to the atmosphere at room temperature. SiO_2 can be used as an electrical insulator, it has an electrical resistivity larger than 10^{16} Ωm and a band gap of 9 eV. SiO_2 is also used as a diffusion barrier (see chapter 4) in microelectronics. This chapter goes through the oxidation process and the technology used to oxidize Si wafers.

3.1 Oxidation Process

There are two ways to oxidize Si, wet and dry thermal oxidation. By exposing the Si surface to oxygen gas (dry process) or water vapour (wet) at high temperatures ($800°C - 1200°C$). Both oxygen gas and water vapour can easily diffuse through the native SiO_2 and react with the underlying Si surface at high temperatures. The SiO_2 also consumes the underlying Si during the process and therefore there is about 54% SiO_2 on top of the original Si surface and 46% underneath, see figure 3.1.

Figure 3.1: Oxidized Si wafer with 54% SiO_2 ontop of the original surface and 46% SiO_2 underneath.

The reaction for dry and wet oxidation are

$$Si + O_2 \rightarrow SiO_2 \qquad (dry) \tag{3.1a}$$

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \qquad (wet) \tag{3.1b}$$

The thickness of the oxide can be controlled by tuning parameters that affect the growth rate. Factors such as temperature, time, crystal orientation, pressure and impurities all affect the thickness of the oxide. Wet oxidation has a faster growth rate and is often used for thicker oxides for applications such as masking (see chapter 2). Dry oxidation, which is slower will grow a higher quality oxide instead and can be used for gate oxide. Figure 3.2 shows growth rate depending on time and temperature for the ovens used in the MC2 cleanroom at Chalmers.

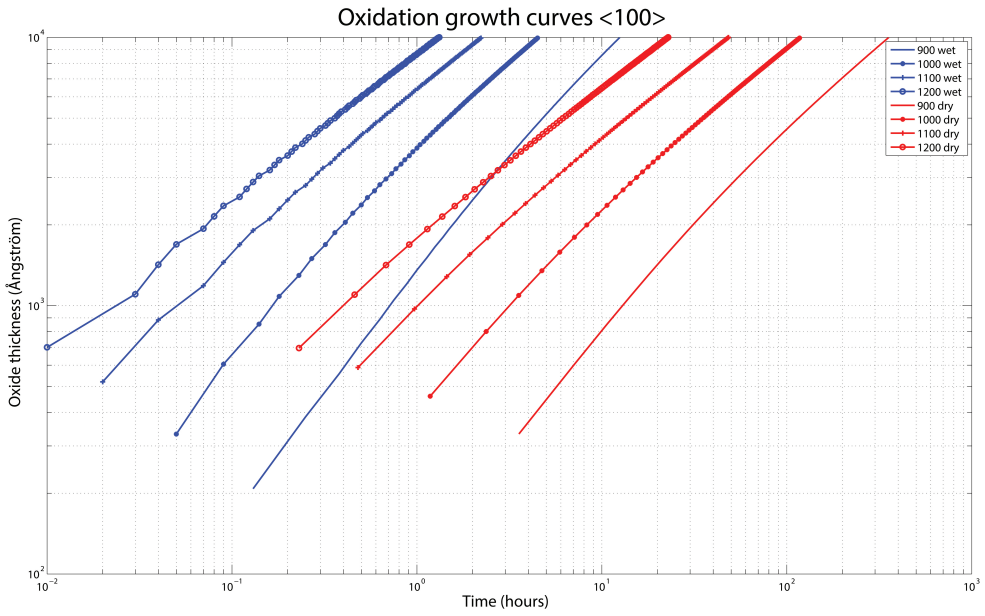
3.2 Oxidation Technology

3.2.1 Furnaces

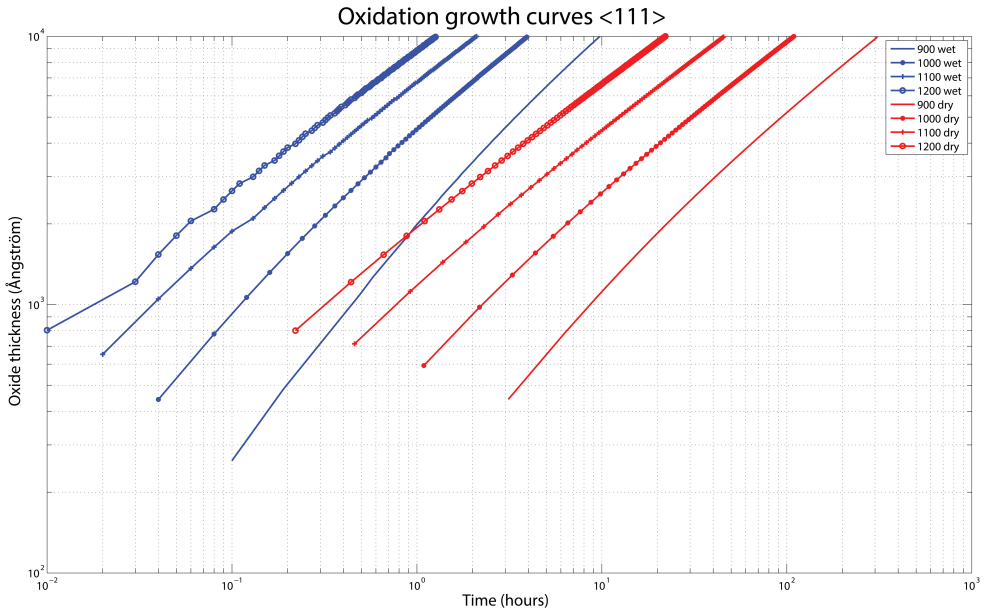
The Si wafers are stacked in a quartz boat (a rack made out of quartz). Quartz has a high melting temperature over 1500 $^{\circ}C$ and is a suitable material for these high temperature processes. The boat with the Si wafers are slid into a quartz tube inside the furnace (figure 3.3). The furnace is heated by resistance heating divided into three zones. The temperature is slowly increasing, to avoid cracking of the quartz, until it reaches the desired oxidation temperature. During dry oxidation, oxygen gas is pumped into the chamber allowing the Si to react with it as in 3.1a and SiO_2 is formed, figure 3.3a. During wet oxidation a carrier gas (O_2, Ar or N_2) goes through a chamber of boiling water and takes with it water vapour inside the furnace and the reaction in 3.1b takes place, figure 3.3a. When finished, the supply gas is turned of the furnace is slowly cooled down.

3.2.2 Rapid Thermal Oxidation

As semiconductor devices become smaller, the movements of impurities due to an increase in temperature becomes more crucial. When the device is heated for a long time the impuritiy profile can change which is undesirable for small devices, this also affects the electrical properties of the device. When thermal oxidation is done with furnaces there is long ramping time and a long process time due to the slow temperature transition. Therefore rapid thermal oxidation can be used. Rapid thermal oxidation systems can have a ramping time from $10-350\ ^{\circ}C/s$ compared to oxidation furnaces that have a ramping time of $0.1\ ^{\circ}C/s$. The systems consist of an array of lamps that heats the wafer optically. To be able to determine the existing temperature within the system various kinds of pyrometry is used. The rapid thermal oxidation process is on a single wafer process compared to the oxidation furnaces which can take several wafers at a time.

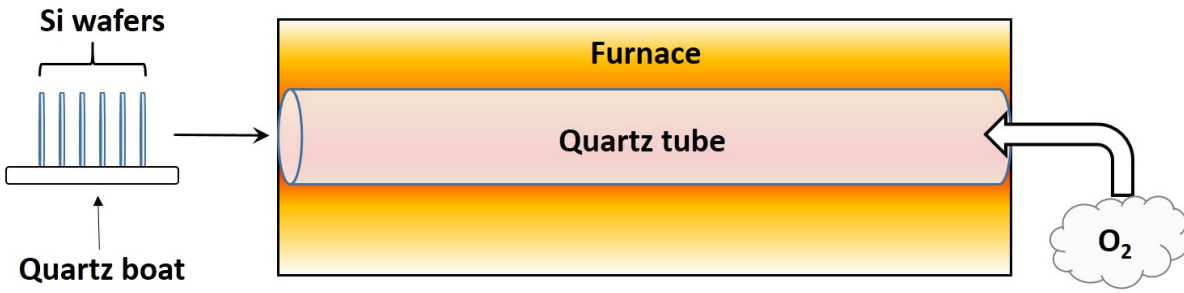


(a) Oxidation growth for a 100 Si wafer.

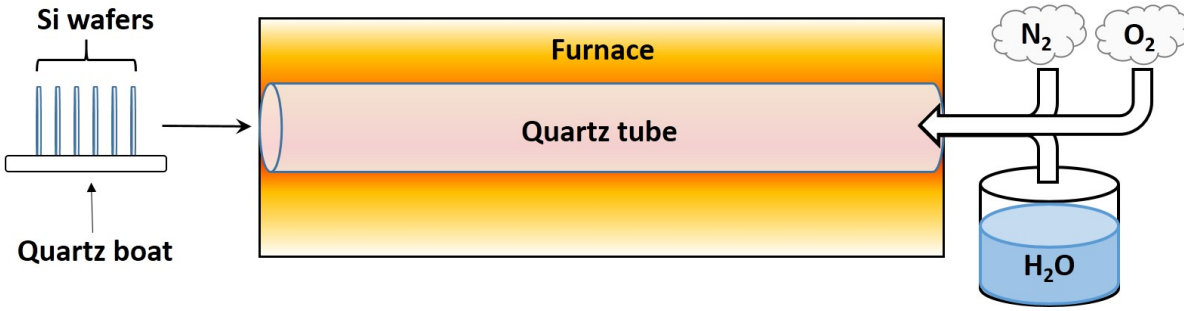


(b) Oxidation growth for a 111 Si wafer.

Figure 3.2: Wet and dry oxidation growth vs. time depending on temperature and crystal orientation.



(a) Dry oxidation furnace.



(b) Wet oxidation furnace.

Figure 3.3: Oxidation furnaces.

Chapter 4

Doping

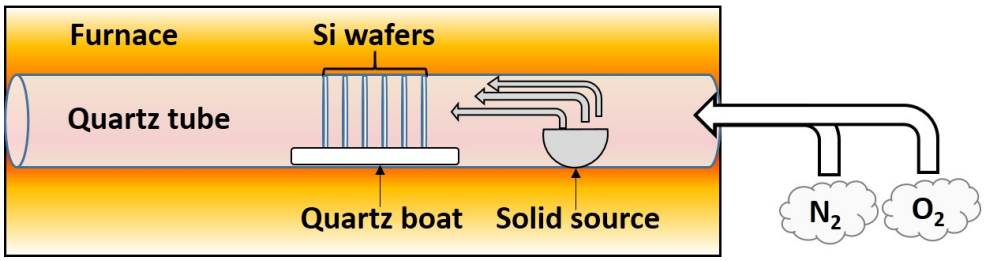
To be able to control or enhance the electronic properties of semiconductors one uses doping. Doping is when introducing an impurity, typically an atom with fewer or more electrons in the outer shell than the semiconductor to increase the electron or hole concentration making it n-type or p-type respectively. The semiconductor can be doped during the bulk crystal growth by introducing the dopant (together with the precursor gases), thus doping the entire crystal. If one wants to dope specific areas of the wafer diffusion or ion implantation are two other methods used for this purpose.

4.1 Diffusion

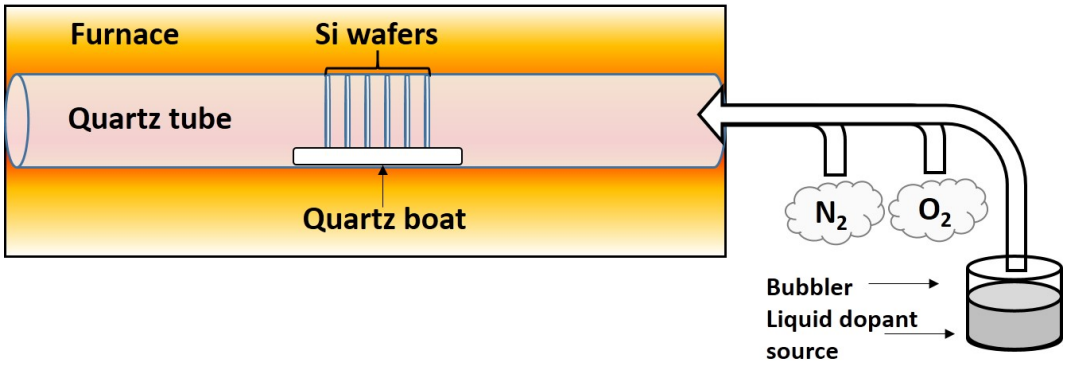
When particles from a region with a high concentration moves to a region of lower concentration it is called diffusion. Imagine having a container with a wall separating ink and water, when the wall is removed the random motion of the ink will result in a net motion towards the clear water, as time passes the ink is completely diluted by the water and a steady state is reached.

There are three ways of diffusion, the first is empty space diffusion where the impurity set in an empty space in the lattice, the second is interlattice diffusion, when the impurity moves between the atoms of the lattice and the third is when the impurity switches place with an existing atom in the lattice.

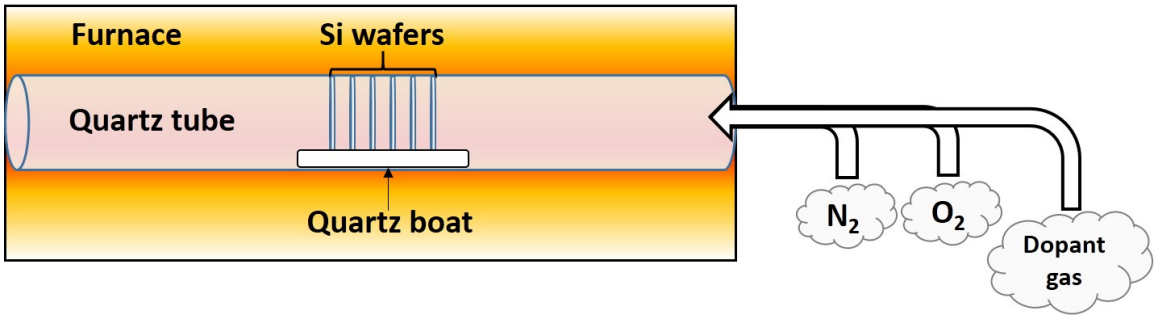
When doping silicon with diffusion, the Si wafer is placed in a quartz boat and slid into a furnace, similar to the oxidation process in chapter 3. Inside the chamber the wafer is exposed to the impurity source. The unprotected Si will have a high concentration of impurities outside it and none inside. When the temperature is elevated to $900 - 1200\ ^{\circ}C$ the impurity can move into the Si. To protect certain areas from being doped, SiO_2 is used as a barrier layer, see chapter 2. SiO_2 is not immune to the diffusion, however the diffusion is much slower compared to Si. There are three sources of impurities, solid, liquid and gas. A solid source is placed in the furnace together with the wafers, either as discs between the wafers or in a platinum boat as in figure 4.1a. When the solid source is heated it diffuses into the atmosphere and together with a carrier gas it is spread out and reach the wafers. Figure 4.1b shows the setup for a liquid source, where the liquid is in a bubbler and heated to a gas where it together with a carrier gas is distributed in the atmosphere. In figure 4.1c the source is already in a gaseous form and will with the help of the carrier gas it flows into the chamber allowing the source to diffuse into the wafers.



(a) Diffusion furnace with a solid source.



(b) Diffusion furnace with a liquid source.



(c) Diffusion furnace with a gaseous source.

Figure 4.1: Different types of diffusion furnaces.

This first step with a constant source is called the pre-deposition step. The diffusion continues until the surface concentration at the wafer is equal to the concentration outside the wafer surface. The doping is very shallow and therefor there is a follow up step called drive-in where the supply of dopants is cutoff and the temperature is increased, driving the impurities deeper into the wafer. The drive-in step gives better control of the dopant profile and depth by controlling the duration time and the temperature.

4.2 Ion Implantation

Ion-implantation is a doping method that uses a high-voltage particle accelerator to shoot ions into the wafer. The ion implantation system is schematically shown in fig-

ure 4.2. The impurity we want to use to dope the wafer is made into ions. The ion source produces a plasma with both the wanted impurities as well as unwanted side products. The ions are accelerated into an analyzing magnet, which bends the path of the ions. The wanted ions are sent through a slit, however the unwanted ions which are lighter or heavier will collide with walls around the slit. Thereafter the wanted ions passes through a high-voltage accelerator which accelerate the ions to the desired speed needed to shoot into the wafer. The beam is the focused through a lens and controlled with x- and y-plates so that the beam can be scanned over the wafer. The wafer can be scanned also by moving the wafer or by utilizing both the x-y plates and moving the wafer at the same time. Before the beam hits the target it is slightly bent to avoid neutral particle from hitting the wafer, these neutral particle will be caught by the beam mask.

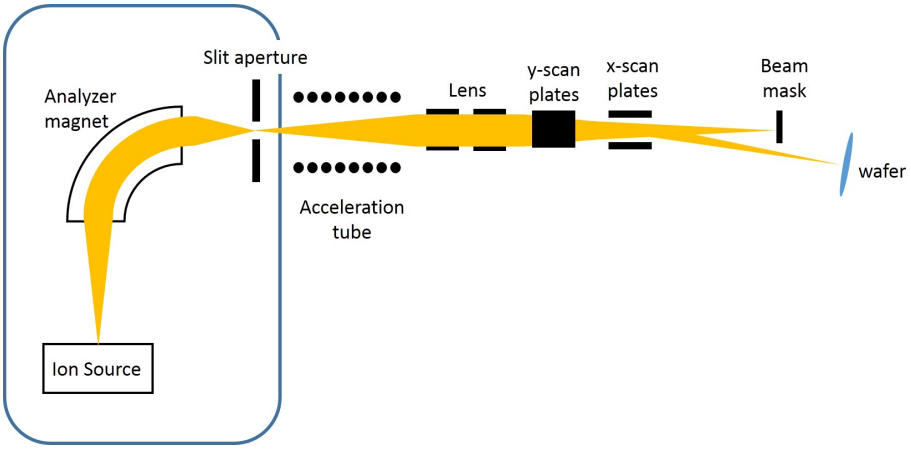


Figure 4.2: Schematic drawing of an ion implanter.

Chapter 5

Film Deposition

There are many uses for film deposition in microfabrication. The film could be oxides, metals or even organic materials. In surface micromachining the film is often used as electronic components such as contact pads, interconnect, gates, gate oxides etc. Films can also be used as hard mask (barrier layers, chapter 2), e.i. patterns that is not effected by the etchant when etching deep into the wafer. There are many deposition techniques, in this chapter four types of methods are discussed, evaporation, chemical vapor deposition and sputtering. Also in this chapter a bottom-up technique called epitaxy is discussed where the layer is grown on the wafer.

5.1 Evaporation

Evaporation is a quite straight forward process where the source which is located underneath the wafer is heated at low pressures until it is vaporized. The vapour then ascends towards the wafer and is deposited on the wafer surface as a thin film.

In this section two methods of doing so will be presented, Filament Evaporation and Electron Beam Evaporation. Filament evaporation (figure 5.1) is when the source is placed on a filament (tungsten, quartz, graphite etc). The filament is heated by resistance heating until the source is melted down and parts of it becomes vapour. The chamber containing the source and the wafer has been evacuated so that the vapour can descend freely towards the wafer. Sometimes the wafer is heated to improve adhesion of the thin film on the wafer. Filament evaporation is quite simple but has a high level of contamination. With electron beam evaporation a high power e-beam is focused on the source until parts of it is vaporized. Here the deposition is controlled by the current and the energy. A schematic view of the setup can be seen in figure 5.2.

When depositing by evaporation on a patterned surface, shadowing can occur. That is when features close to each other on the surface is obstructing the vapour from covering the intermediate surface between them, see figure 5.3. Sometimes this affect can be used as a benefit but if unwanted the wafer can be rotated to avoid this effect.

5.2 Chemical Vapour Deposition

Chemical Vapour Deposition (CVD) forms a film from one or several gases that react with each other or decompose at the wafer surface, resulting in a thin-film on the wafer.

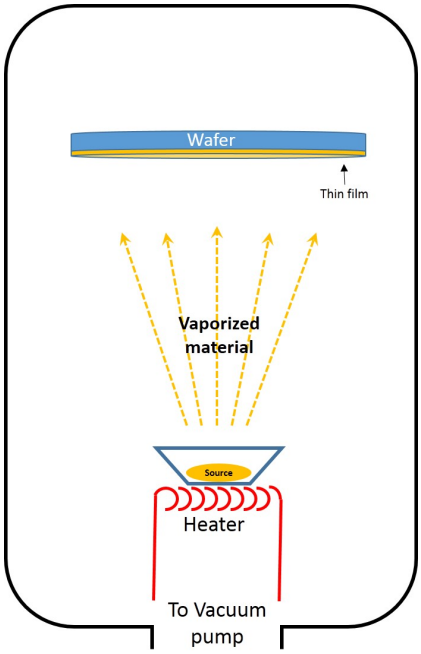


Figure 5.1: Filament evaporation chamber

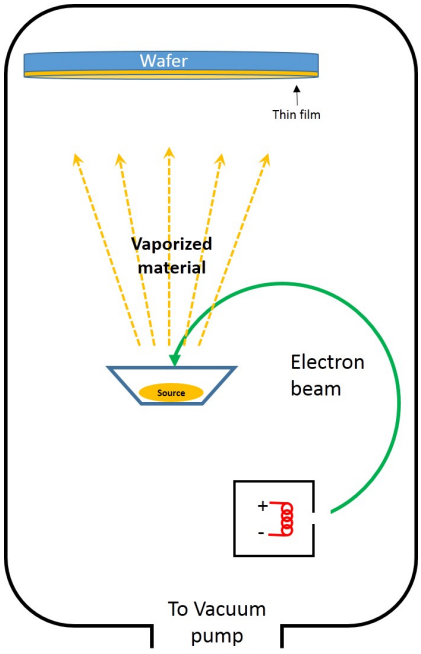


Figure 5.2: E-beam evaporation chamber.

CVD can also be used to synthesize carbon nanotubesThere are several different CVD processes, in this section three of them will be described.

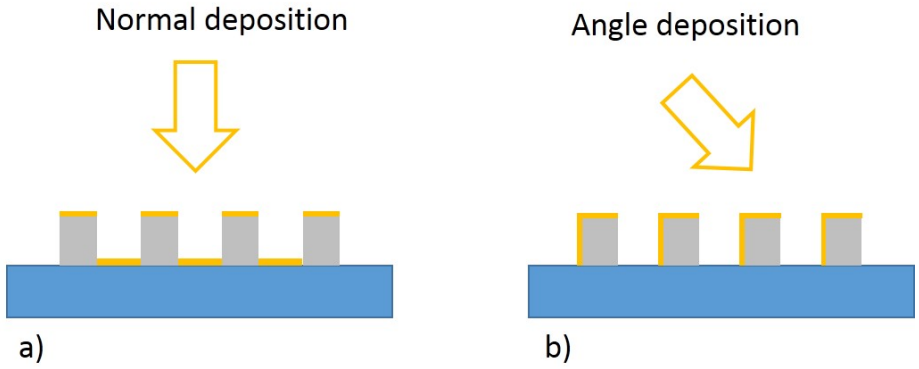


Figure 5.3: a) Film topology, when depositing from a normal direction. b) Film topology, when depositing from an angle.

Atmospheric-pressure Chemical Vapour Deposition (APCVD) also called in general CVD can be used to deposit oxides. The gases are flown at the wafer and the wafer is heated to assist the reaction on the surface at normal pressure. The process has the benefit of a high wafer throughput but the step-coverage is low.

LPCVD (Low-Pressure Chemical Vapour Deposition) has vacuum during the process. The low pressure gives a better step coverage due to the limitation of the movement of the particles and therefore the spreading is because of collisions instead. LPCVD is a high temperature process where the gases enter at one side of the furnace tube and exited at the other end. The process has the advantage of processing several wafers at a time but the inner walls of the tube are covered with the thin-film and needs to be cleaned on a regular basis.

PECVD (Plasma Enhanced Chemical Vapour Deposition) has a chamber similar to the one in section 6.2. Here the gas is inserted between the top electrode and the lower electrode, where the wafer is placed. An RF signal is applied creating a plasma of the gas. The process is a low temperature process which allows deposition on metals, however wafers needs to be loaded manually which is a disadvantage.

5.3 Sputtering

Sputtering is a deposition technique that bombards the source with ions and releases atoms that is deposited on the wafer. Most sputtering machines are magnetron sputters which has magnetron tubes attached to the target. The magnetron creates an electric and magnetic field that guides the particles to the wafer surface. With a power source the target can have a negative voltage of around $-300\,V$. This attracts positive ions at a high speed towards the target. If the energy is high enough at impact the bound atoms of the target will emit, hitting the substrate. Not all ions will have this effect some will be buried inside the target causing defects and some will create secondary electrons which will sustain the glow discharge. Magnets beneath the target helps keep the secondary electrons close to the target. The electrons will spiral around the magnetic field. The plasma is easily ionized and the sputter rate is enhanced. This also allows for lower pressures inside the chamber.

The target is rotated above the substrate to enable uniformity of the deposited layer.

The step coverage for sputters are better than evaporation techniques because of the different impact angles. Both the target and the substrates are in a low pressure chamber with a pump connected to it for evacuation. Of the five magnetron cathodes in the sputter (FHR MS 150) in the MC2 cleanroom three are used for DC sputtering and the rest for RF. RF sputtering is good when using isolating substrates to avoid charge build-up. The gases used are Argon, Nitrogen and Oxygen.

The targets used are Aluminium, Titanium and Gold where the Titanium is used to get better adhesion for the gold. The different deposition rates for the FHR MS 150 can be seen in table 5.1.

Table 5.1: Deposition rate for different materials

Material	Al $8 \cdot 10^{-3}$ *mbar*, 1 *kW*	Ti $5 \cdot 10^{-3}$ *mbar*, 1 *kW*	Au $5 \cdot 10^{-3}$ *mbar*, 0.2 *kW*
Deposition rate	2nm/sec	1.1 nm/sec	1.2 nm/sec

5.4 Epitaxy

Epitaxy is when a crystalline layer is grown on top of a crystalline substrate, the new crystalline layers lattice is an extension of the underlying crystalline lattice. Most commonly it is used to deposit a layer with a different doping than the underlying layer. There are three types of epitaxy methods, Vapour-Phase Epitaxy (VPE), Liquid-Phase Epitaxy (LPE) and Molecular Beam Epitaxy (MBE).

The most common method, VPE is a type of CVD where a gas containing the a compound of the desired material is pumped into a heated chamber, where it then reacts at about $1200°C$ with the substrate and new crystalline layers are grown. For Si substrates, gases such as $SiCl_4$, SiH_4, SiH_2Cl_2, $SiHCl_3$ are used. To dope the new crystalline layer, impurities are introduced together with the deposition gas.

LPE is a technique where the source is in liquid form, often by being melted. The substrate is in contact with the liquid source under controlled temperatures and acts as a seedlayer, the material crystalizes directly upon contact. Here is a nice animation (http://www.microelectronique.univ-rennes1.fr/animation/animepitaxie.htm). of the process. Growth rates for LPE typically ranges from 0.1 $\mu m/min$ to 1 $\mu m/min$.

A molecular-beam is a thermal beam of atoms/molecules. The solid source for the beam is heated in a crucible called Knudsen effusion cell until it directly goes into the gaseous state without it becoming a liquid first. The gas goes through a narrow opening into a high-vacuum chamber as a beam until it reaches the heated substrate $(400 - 900°C)$ to which it reacts to and a crystalline film is grown. Reflection high energy electron diffraction (RHEED) guns are ued to monitor the film thickness and control the openings at the source, so that the thickness can be controlled with atomic precision. A good schematic image of the setup can be seen in figure 5.4.

This is as pure method due to the high vacuum but a relative slow growth rate. In the MC2 cleanroom the MBE system has a growth rate of 1 $\mu m/h$.

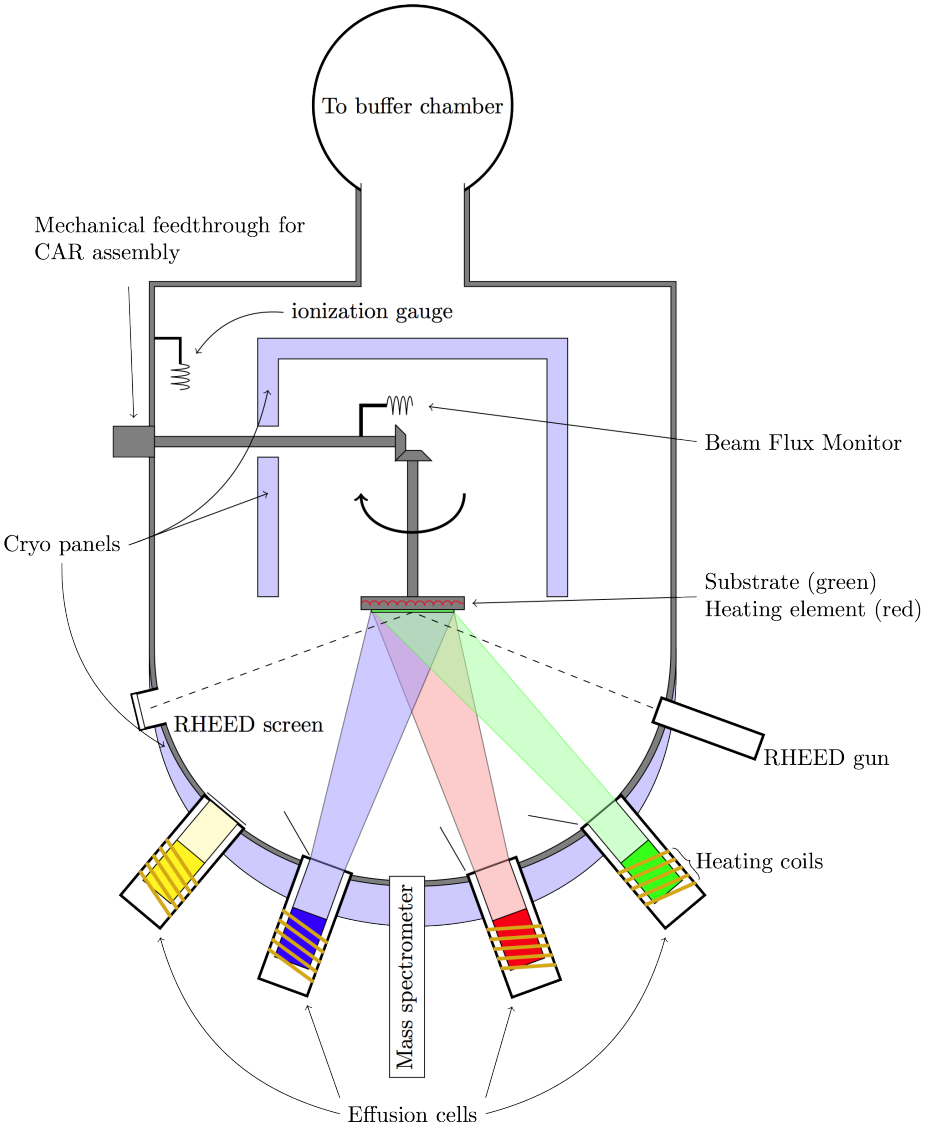


Figure 5.4: Image curtesy of Vegar Ottesen, wikipedia; A simple sketch showing the main components and rough layout and concept of the main chamber in a Molecular Beam Epitaxy system Molecular Beam Epitaxy growth chamber.

Chapter 6

Etching

Etching is used to remove material by immersion in a solution (wet etching) or with a plasma (dry etching). Entire wafers can be etched but often it is used to etch certain areas of the wafer. This is done by having a patterned protective film (see hard mask in chapter 2) that will not be etched in the same process or has a high selectivity compared to the material that is to be etched. There are two types of directional etching, isotropic and anisotropic i.e. when the etchant etches equally much in all direction respectively when the etchant etches more in one direction than the others.

6.1 Wet Etching

Wet etching of thin-films such as SiO_2 and Al are isotropic. To etch SiO_2 buffered oxide etch (BOE) is commonly used, also called BHF because the solution contains HF. The etching is done at room temperature and can be facilitated by agitation. HF is very dangerous if in contact with your skin, it will deplete the bone from calcium. That is why it is diluted when used but can still cause damage at contact. BOE has also a more controllable etch rate of $10-100$ nm/min. How the oxide was done can also affect the etch rate. Oxide made from dry oxidation (see section 3) etches slower than oxide from wet oxidation. For wet etching of Al a compound with the ratio of 16:1:1:2, phosphorus acid: acetic acid: nitric acid: DI is used in the MC2 cleanroom. This compound has a etch rate of 200 nm/min.

Anisotropic wet etching utilizes the crystal orientation, where some orientations etches faster than other. This is quite common for Si bulk etching. For example when etching Si with KOH the <100> surface etches 400 times faster than the <111> surface, at $80^{\circ}C$ a 35% KOH solution has the etch rate of 75 $\mu m/h$. If working with doped areas, mobile potassium ions can be introduced into the SiO_2 and may cause problems. EDP (Ethylenediamine pyrocatechol) does not etch SiO_2 at all but it is highly corrosive. EDP has a selectivity of 17:1 for <100>:<111> and an etch rate of 28 $\mu m/h$, nominal operating temperatures around $110^{\circ}C$. TMAH (Tetramethylammonium hydroxide) which can also be used for anisotropic wet etching of Si has a selecticity of 37:1 between <100> adn <111> and normal operating temperatures are $70-90^{\circ}C$ and it has an etch rate of 20 $\mu m/h$.

6.2 Dry Etching

Dry etching is done with the help of a plasma. The basic principle of plasma etching is by supplying a gas into a vacuum chamber. Inside this vacuum chamber ions are accelerated through the gas due to an electric field. When the ions are accelerated through the plasma they collide with the gas molecules. The energy from the collisions ionizes the gas more and increases the amount of ions and electrons. This continues until breakdown occurs, this voltage is called the Townsend discharge. The ions from the gas are then directed towards the wafer and either mechanically or chemically by reactions remove atoms from the wafer.

The plasma can be created in different ways, here we will discuss inductive coupled plasma (ICP). Inductive coupled plasma is induced by a coil around the chamber. Through the coil an RF current causes an alternating magnetic field. The changing magnetic field produces an alternating electric field circulating in the gas. The fast moving electrons collide with the slow ions and produce more ionizations. ICP plasma generates relatively high density plasma.

Plasma etching is somewhat of an isotropic process but there are ways to achieve anisotropic etching by using e.g. the Bosch process. The Bosch process is an alternating process between isotropic plasma etching and applying a passivation layer. First isotropic plasma etching with the gas SF_6 is done for a certain etch time. Then a fluoropolymeric passivation layer from C_4F_8 is deposited which covers all sides of the now isotropic trench in the wafer. When etching again the plasma is mostly focused downward and the plasma etches through the passivation in the bottom but the passivation layer on the sides are not that much affected. When alternating between etching and passivation a scalloped wall is developed. The unevenness of the walls depends on for how long each etch step is and how much passivation is used. The amount of passivation is determined by how long the passivation time is.

The Bosch process is a deep reactive ion etching (DRIE) process. Four parameters are tuned to achieve the desired structure. The four parameters are etch time, passivation time, pressure and platen power. The etch and passivation time as mentioned earlier affects the surface of the walls and anisotropicity. By increasing the platen power the electric field will increase, this results in transmitting more energy to the electrons. The etch will become more mechanical than chemical and the hard-masks selectivity is decreased. The increase of the electric field will also increase the speed of the ions toward the wafer. The pressure in the chamber is controlled by a throttle valve and how much it is opened. The increase of pressure have two opposite effects. The first is that there are more ions that can collide with each other, which leads to more free electrons. However the mean free path of the electrons before collision is reduced and the electron has less energy before colliding. The choice of pressure is therefore a trade-off.

Chapter 7

Device Fabrication Examples

In this chapter a piece from the book *Semiconductor Device Fundamentals* by *Robert F. Pierret* has been borrowed to show device fabrication examples for devices such as the pn-junction diode.

4.2.1 *pn* Junction Diode Fabrication

Figure 4.15 graphically summarizes the major processing steps in the formation of a *pn* junction diode. The starting point is a flat, damage-free, single-crystal Si wafer. It is assumed that a preclean has removed all particulates, organic films, and adsorbed metal ions from the semiconductor surfaces. For this particular illustration we further assume the wafer is *p*-type, having been uniformly doped with boron during the formation of the crystal.

The initial steps in the process flow are in preparation for a subsequent phosphorus diffusion. First a thermal oxide is grown that will serve as a diffusion barrier. The oxide thickness must be comfortably greater than the projected masking thickness. Step 2 is a lithography process performed to open "diffusion" holes in the oxide that will eventually become the positions of the *pn* junction diodes. Specifically note that the Step 2 illustration in Fig. 4.15 assumes the use of a positive photoresist.

After a proper clean-up the wafer is next inserted into a phosphorus predeposition furnace and subsequently into a phosphorus drive furnace. The net result, as pictured in Step 3 in Fig. 4.15, is the formation of n^+-p junctions in surface regions not protected by the oxide. (The + in n^+ indicates a very high doping.) By way of clarification, some oxygen is required during the phosphorus predeposition as noted in the diffusion discussion. Also, the drive may be performed in an oxidizing atmosphere to minimize out-diffusion. Thus, to reopen the oxide holes, a subsidiary lithography step, not shown in the simplified process flow of Fig. 4.15, is usually necessary after diffusion.

The final steps facilitate connecting the device to the "outside world." Sputtering or possibly evaporation of Al yields a thin metal film over the entire surface of the wafer as pictured in Step 4 of Fig. 4.15. A lithography process, Step 5 in Fig. 4.15, is then performed to remove excess metal external to the area of the diffused junction. Normally a low-temperature ($\leq$500°C) anneal would also be performed to promote a low-resistance contact between the metal and Si.

With the completion of the metallization contact, the diodes become functional across the wafer. To produce commercial diodes, a diamond-edged saw would be used to cut the wafer into pieces containing a single device. (A wafer piece containing a single device or IC is called a *die*.) A large area metal contact is then made to the back of the die, a lead attached to the top surface contact, and the device encapsulated in protective plastic or hermetically sealed in a metallic package.

4.2.2 Computer CPU Process Flow

In this subsection we examine a fabrication process flow that has been used by Intel Corporation to produce computer CPUs and other ICs. The process flow description and associated figures are a direct excerpt, reprinted with permission, from *Components Quality and Reliability 1991/1992*, Intel Corporation, © 1990. No changes have been made to the excerpted material except for a renumbering of the figures and a modification of the figure captions. Figure 4.16, reproduced from the cited reference, displays a simplified block dia-

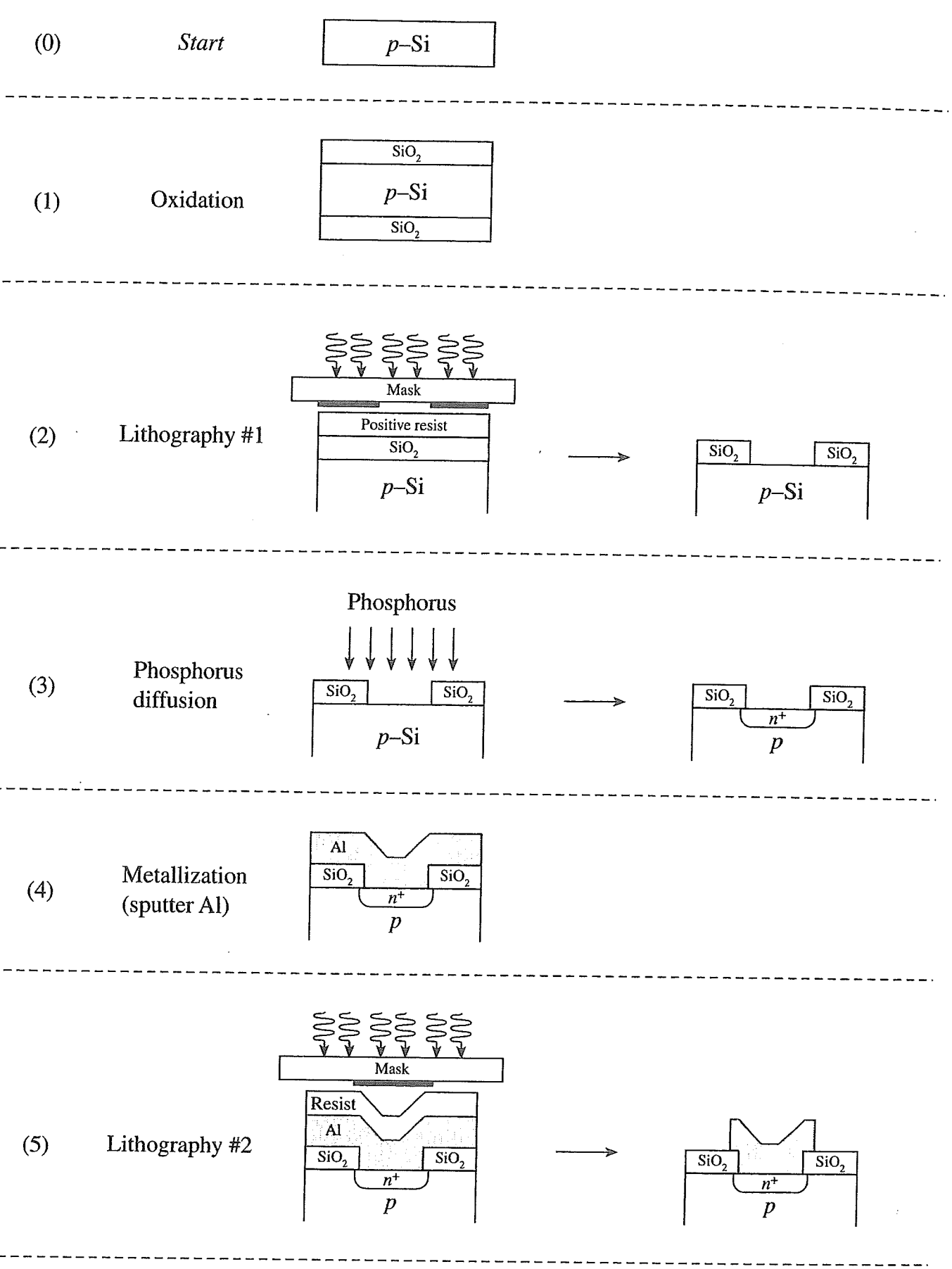


Figure 4.15 Graphical summary of the major processing steps in the formation of a *pn* junction diode.

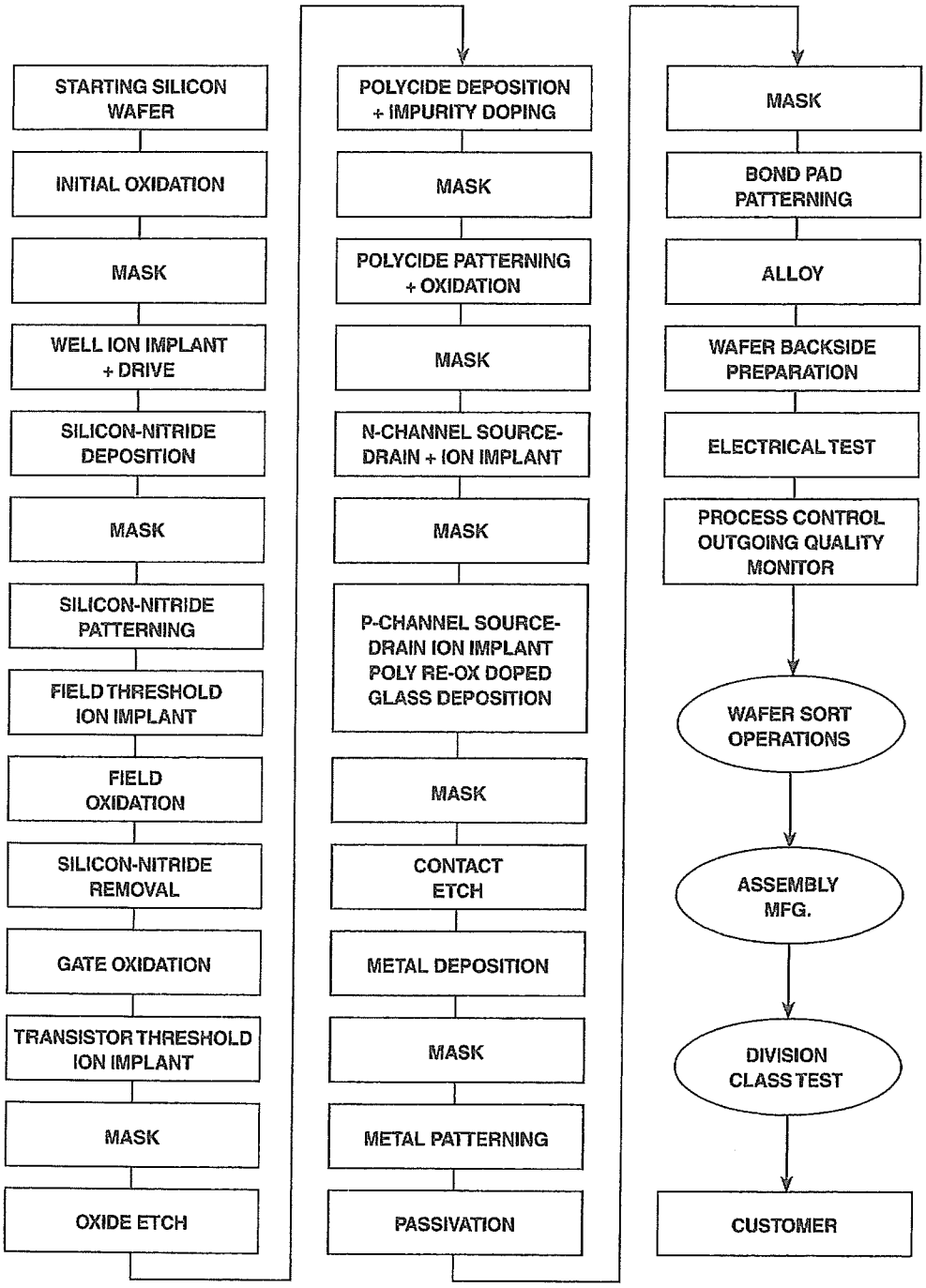


Figure 4.16 Simplified block diagram of the single poly, single metal, CHMOS process flow.

gram of the overall process flow. Figure 4.17, which is correlated with the text description of the component processes, shows cross-sectional sketches of the IC structure at various stages of construction.

Although most of the terms employed in the process description will be familiar to the reader, a few need to be clarified. For one, the fabrication sequence is referred to as a single poly, single metal, CHMOS process flow. "Poly" is short for polycrystalline Si. CHMOS stands for Complementary High-density Metal-Oxide-Semiconductor—a type of fabrication technology used to produce MOS transistors. "Single poly, single metal" indicates that one level of heavily doped polycrystalline Si and one level of metal are used to contact

and interconnect the MOS devices. Text references are also made to "wet" and "dry" etches. Wet etching is the familiar dissolution of a material, such as SiO_2, in a liquid chemical bath. Dry etching is the removal of a material using a plasma-enhanced gas-phase reaction.

Finally, the following process flow description is intended to be "looked over," not digested. At this point in the development, the reader is not equipped and not expected to understand the intricacies of either the processing or the IC structure.

---

1. **Starting Silicon Material and Well Definition** [Fig. 4.17(a)] To start CHMOS device production 150 mm (6″), high-resistivity, ⟨100⟩ orientation, single crystal, p-type (Boron doped) silicon wafers are used. P-type silicon is required to create n-channel transistors. To create p-channel transistors, necessary for CHMOS devices n-type (arsenic or phosphorous doped) silicon regions (n-wells) are implanted. The wafer is masked, then implanted to create p-type and n-type silicon regions on the same wafer. The n-well provides the background doping for the p-channel transistors while the p-type, start material (protected from the implant by the unexposed photoresist) serves as the background doping for n-channel transistors. A high temperature drive cycle completes the formation of the well by thermal dopant transition.

2. **Field Threshold Implant and Field Oxidation** [Fig. 4.17(b)]. Nitride (Si_3N_4) is deposited, masked, then etched. The etched nitride regions define the location of the field threshold ion plant [Fig. 4.17(b)] and the locations where oxide SiO_2 is permitted to grow during field oxidation [Fig. 4.17(c)]. Areas where nitride remains mask (prevent) oxide growth. These regions are where transistors will be built. The thick (approximately 6000 Å) field oxide isolates adjacent transistors in order to prevent electrical interactions. After field oxidation, the nitride mask is removed.

3. **Gate Oxidation** [Fig. 4.17(d)]. A thin thermal oxide is grown across the wafer. The portions of this oxide remaining after subsequent processing will provide the required gate oxide for the MOS transistors. Device performance is closely related to the growth of a dense, high-quality gate oxide.

4. **Transistor Threshold Ion Implant** [Fig. 4.17(d)]. The boron implant adjusts the threshold voltage (Vt) of p-channel and n-channel devices to the desired level. Thick field oxide prevents the boron from penetrating into the isolation regions.

5. **Polysilicon-to-Diffusion Contacts** [Fig. 4.17(e)]. Openings are defined in the thin gate oxide region where contact between poly conductors and diffused regions in the silicon substrate (buried contacts) is required.

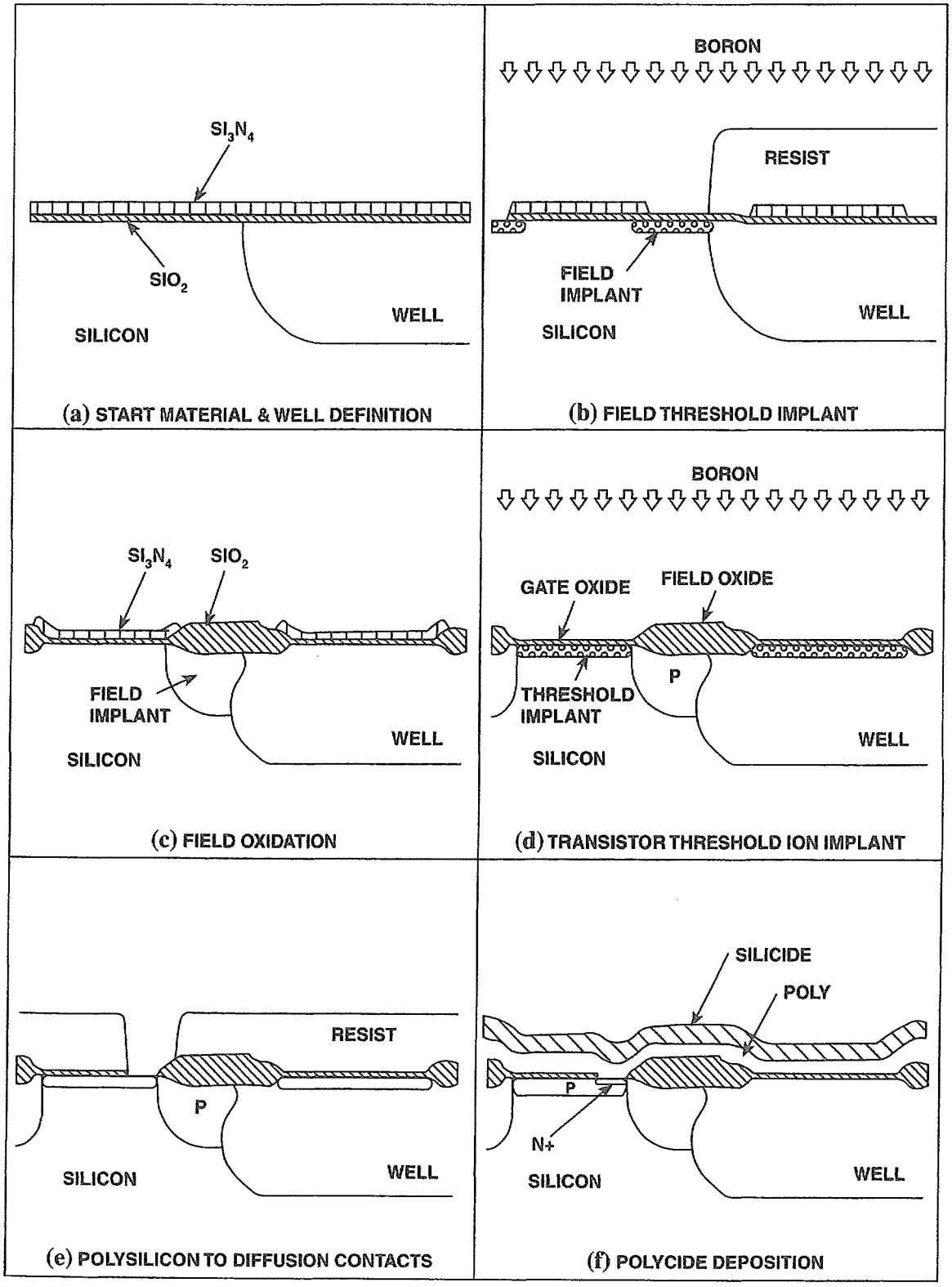


Figure 4.17 Cross-sections through the CHMOS structure at select points in the process flow.

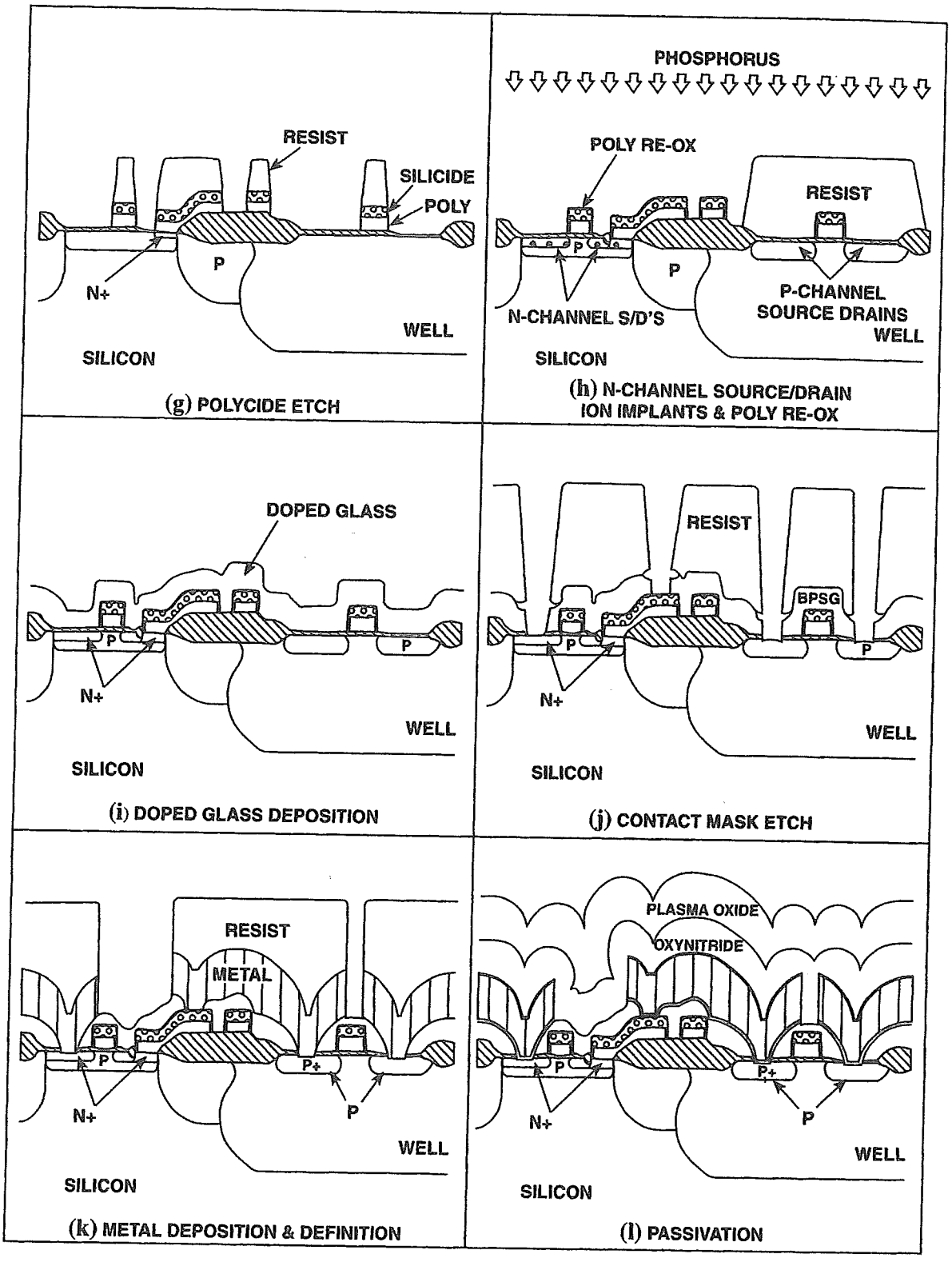


Figure 4.17 *Continued.*

6. **Polycide Deposition, Impurity Doping, Patterning and Oxidation** [Fig. 4.17(f)]. A polycrystalline silicon layer, about 1500 Å thick, is deposited over the entire wafer by CVD techniques. The polysilicon is subsequently doped with phosphorous via gas-source diffusion techniques for conductivity. The phosphorous is diffused through the poly and into the substrate, minimizing the resistance of the buried contact. About 1500 Å of silicide is conformally deposited on the doped polysilicon. Silicide is used in small geometry transistors to increase device performance speeds. The polycide stack is defined by plasma dry etch techniques with resist acting as the mask [Fig. 4.17(g)]. The polycide stack is oxidized to protect the transistor gates.

7. **Source and Drain Implant and Poly Re-Ox** [Fig. 4.17(h)]. The remaining polycide stack, thin oxide over the poly, field oxide and resist provide a mask for p-channel and n-channel source-drain implants which occurs at this point. (This technique is commonly known as a "self-aligned source/drain" process, since the source and drain are aligned directly to the gate, which defines their location relative to the channel area.) All remaining poly oxide is then removed and the poly re-ox step performed. The re-ox step is a high-temperature thermal oxidation step which drives the source-drain implant into the silicon, provides a high-integrity dielectric on the polysilicon (essential in a double poly process) and grows an oxide on the exposed source-drain regions to prevent dopant out-diffusion during subsequent phosphosilicate glass deposition and processing.

8. **Doped Glass Deposition** [Fig. 4.17(i)]. A doped (boron, phosphorous or both) silicate glass layer, 5000 Å to 10,000 Å thick, is deposited via low-temperature CVD techniques to provide electrical isolation between the subsequent metal conductor lines and the underlying polycide gates and active device structures. The glass is then prepared for subsequent masking steps.

9. **Contact Mask and Etch** [Fig. 4.17(j)]. Windows in the resist are exposed and opened to define the location of metal-to-polycide and metal-to-silicon contact holes. Depending on the process, contact holes are wet, dry, or wet and dry etched. In a wet/dry combination, the wet etch gives a shallow slope near the top of the contact. This improves metal step coverage. The remaining doped silicon glass is then removed by an isotropic dry etch which leaves the contact sidewalls vertical.

10. **Metal Deposition and Definition** [Fig. 4.17(k)]. Metal conductor layer is sputter-deposited into the wafer and defined. The metal electrically connects the transistors to the outside world. The voltage applied by these metal lines turns the transistors "on" and "off."

11. **Passivation** [Fig. 4.17(l)]. Plasma enhanced CVD techniques are used to deposit a dual film passivation layer over the entire wafer surface. The dual layer consist of an

oxynitride underneath a plasma oxide. The oxynitride provides long-term field reliability, by being designed to be a contamination and moisture barrier. The latter is particularly critical if the dice are to be assembled in plastic packages, plastic itself being a poor moisture barrier. The plasma oxide layer provides handling protection for the wafer and individual devices.

Most of the remaining production-line and testing steps cited in the Fig. 4.16 block diagram are in preparation for eventual IC die separation and packaging. The photograph of a sample CPU die, along with an identification of its functional units, are displayed in Fig. 4.18. The pictured Pentium™ Processor die, fabricated following an upgraded version of the described processing, is approximately 1.5 cm square and contains 3.1 million transistors.

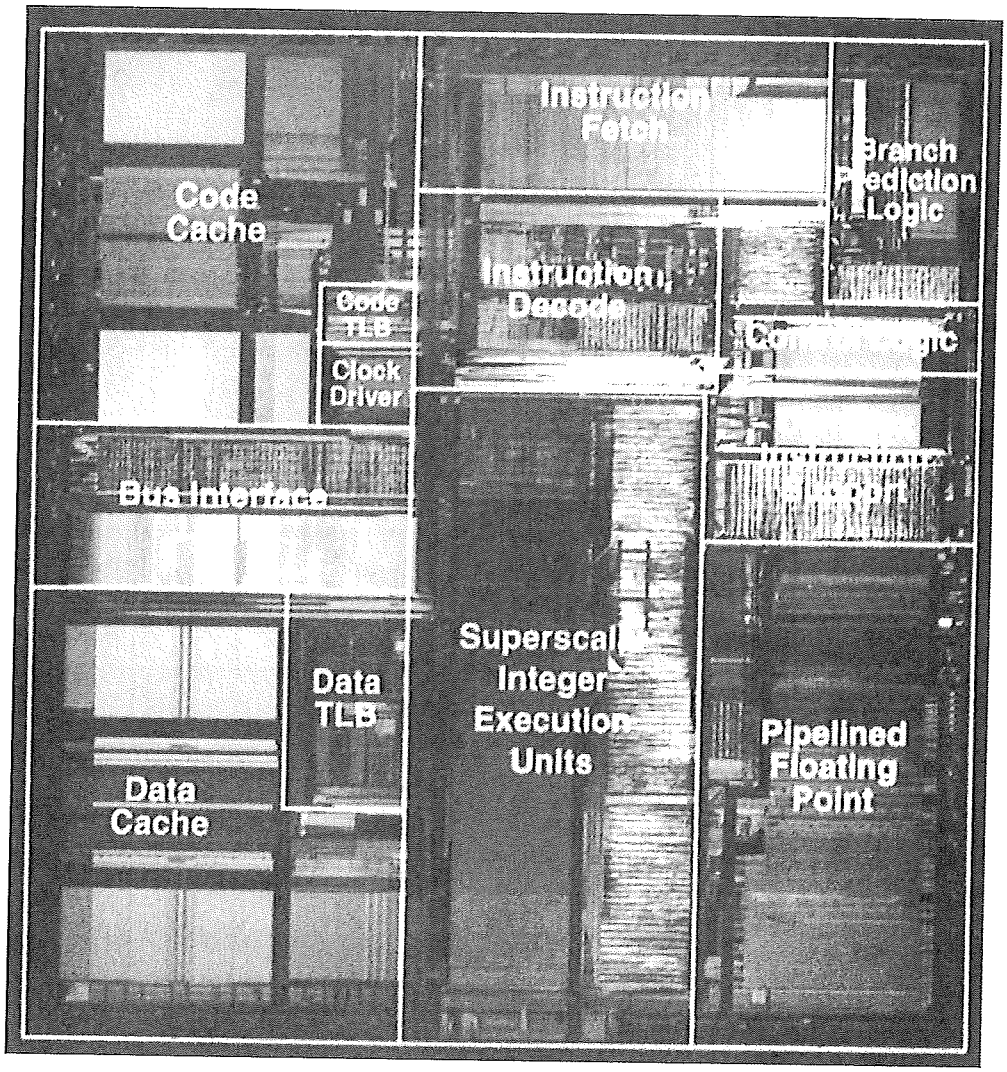


Figure 4.18 The Intel Pentium™ Processor and its functional units. (Photograph and functional unit identification courtesy of Intel Corporation.)